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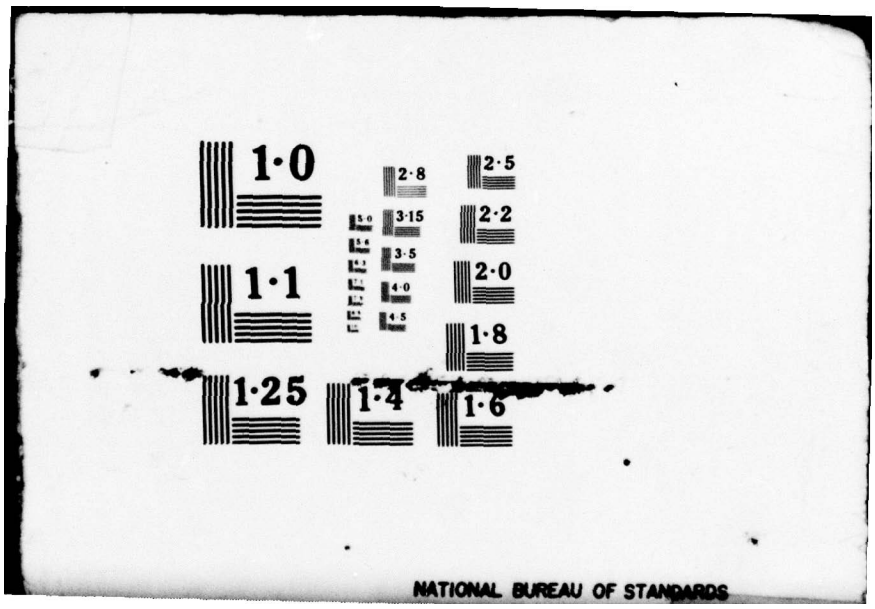
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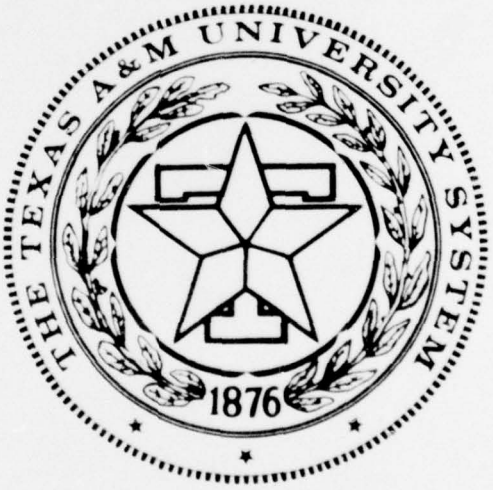

DEPARTMENT OF ELECTRICAL ENGINEERING
College Station, Texas

LEVEL II

2

DSL Research Memorandum 78-03

A Final Report for AFOSR
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A Comparison of Low-Cost Microprocessors for the GPS Receiver Processor

by

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September 26, 1978

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This report compares the floating point capabilities of the LSI-11 Motorola 6800, and projects the capabilities of three recently announced 16-bit processors, the Intel 8086, the Zilog Z8000, and the Motorola 68000.

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Program studies began June 1, 1977 and will be completed on (or about August 31, 1978. Dr. P. S. Noe served as Principal Investigator and was assisted by Dr. S. Suraratrungsi.

Introduction

Since the Interim Report (DSL Research Memorandum 78-02) was completed, three new 16-bit processors have been announced: the Intel 8086, the Zilog Z8000, and the Motorola 68000. Furthermore, an evaluation of the DEC LSI-11 and the Motorola 6800 has been made to provide a more complete spectrum of floating point processing that is available with existing microprocessors.

New High Performance Microprocessors

The Intel 8086, the Zilog Z8000 and the Motorola 68000 are three new 16-bit microprocessors that have been announced in the past 9 months. However, quantitative information has not been released on the Intel 8086.

Zilog claims that the "Z8000 is 5 to 10 times faster than modern 16-bit microprocessors or popular minicomputers such as the PDP 11/34". If this statement is true, it may be possible to improve the Z80A execution times shown in Table I by an order of magnitude (or at least in the 40 μs range) since the Z8000 instruction set will presumably be at least as powerful as the Z80A. It is apparent that the multiply time is not any faster than the Texas Instruments 9900 from Table II. However, the faster add, load, and generally more powerful instruction set will make the Z8000 an excellent candidate for use in a low cost GPS receiver.

The September 1, 1978 issue of Electronic Design contains an article describing Motorola's 16-bit microprocessor, the 68000. This chip will have a powerful instruction set including hardware multiply and divide. A complete comparison with the other 16-bit processors is not possible, however, since the only information regarding execution times is for byte addressing operations as shown in Table II. This value

does, however, give an indication that the 68000 will prove to be very competive with all of the other known 16-bit processors if the other instruction execution times correlate in a linear fashion with the addressing spec. Add/multiply ratios of the Z8000 and TI 9900 would indicate a multiply speed of 6 to 12 μs for the 68000. If this proves to be true it will be a powerful competitor, indeed.

Perhaps a major advantage of the 8086, the 8000, and the 68000 is the large amount of directly addressable memory that is possible with these three processors. The 8086 addresses one M-byte of memory, the 8000 addresses 8 M-bytes, and the 68000 addresses 16 M-bytes of memory. On the other hand, the TI 9900 directly addresses only 32 k-words of 16-bit memory. This fact should not prove to be a great limitation, however, since it is anticipated that the low-cost, C/A code, GPS algorithms will not require more than 32 k-words of memory.

The Motorola 6800 and the DEC LSI-11

To complete the comparison of microprocessors that are in wide use at the present time, the floating point capabilities of the Motorola 6800 8-bit microprocessor and the DEC LSI-11 16-bit microprocessor have been investigated. A graduate course in Floating Point Computation was taught at Texas A&M University in the Summer of 1978 by Dr. Chuck Adams. All students were required to create a floating point processor for the Motorola 6800 for this course. Execution times for benchmark designs and the best design is shown in Table III. These results indicate (along with Table I) that any of the commonly used 8-bit microprocessors can provide a 2-4 sec. fix rate, with the Z-80 being the best of these 8-bit microprocessors.

	Typical Execution Time (ms)				Memory Space Required (Bytes)	Estimated Fix Rate (Sec.)
	FAD	FBS	FMY	FDIV		
8080A	.41	.44	1.9	3.6	528	3.55
Z-80A	.18	.19	.78	1.5	434	2.09
9900	.23	.25	.35	.26	390	1.55
Bit slice Emulator	.05-.08	.05-.08	.2-.4	.4-.7	one of the above	1.11-2.00
AM 9511 with DMA	.014-.088	.015-.088	.042	.043	none	0.2

Table 1. Microprocessors' Performance Comparison

Operation	Data Type	Z8000 at 4 MHz # Inst.	Bytes	Cycles	µs	TI 9900 at 3MHz Inst.	Bytes	Cycle	µs	Motorola 68000 at 4MHz Inst.	Bytes	Cycles	µs
	Byte	1	4	9	2.25	1	2	14	4.67	—	—	—	1.5
LDR,DA	Word	1	4	9	2.25	1	2	14	4.67	—	—	—	
	Long Word	1	4	12	3.00	—	—	—	—	—	—	—	—
	Byte	1	4	9	2.25	1	2	14	4.67				
ADDR,DA	Word	1	4	9	2.25	1	2	14	4.67				
	Long Word	1	4	15	3.75	—	—	—	—		unknown		
	Byte	3	8	87	21.75	1	2	52	17.33				
MULTR,DA	Word	1	4	70	17.50	1	2	52	17.33				
	Long Word	1	4	~350	~88	—	—	—	—				
	Byte					1	2	92-124	31-41				
DIVR,DA	Word		unknown			1	2	92-124	31-41				
	Long Word					—	—	—	—				

Table II. Fixed Point Execution Times for Z8000 and TI 9900

The DEC LSI-11 16-bit microprocessor was considered primarily because the KEV-11 floating point arithmetic unit is available. Through the use of micro-code the KEV-11 completely overcomes the unavailability of hardware multiply and divide on the LSI-11. Whereas floating point software produces execution times corresponding to the 8-bit microprocessors, the KEV-11 obtains execution times superior to all of the other processors except the bit-slice and the AM-9511 processor. The execution times for the LSI-11/KEV-11 floating point processor are shown in Table III.

Cost/Speed Trade-offs

It is apparent from this study that the execution time on the order of one second per fix is possible with several different microprocessors; specifically, the 9900, the LSI-11/KEV-11, the 8080 bit slice emulator, the AM 9511 with any compatible 8-bit microprocessor, and probably any of the three new 16-bit processors: the 8086, the Z8000, and the 68000.

	Benchmark 1 MC6800 "Motorola" typical μs	Benchmark 2 MC6800 "ADAMS" μs	Best MC6800 "YENDREY" typical μs	MC6800 "YENDREY" w.c. μs	LSI-11 Kev-11 μs
+	1900	336-1450	225	275	66
-	2000	344-1458	250	340	66
*	3200	1702-3252	1700	2150	106
/	6600	3252-4602	2500	3500	151
Bytes	700	700	900	900	0

Table III. MC6800 and LSI-11 Floating Point Execution Times

Individual prices for a single 9900 is almost $39.00, the LSI-11-2 with KEV-11 costs $873.00, the AM 9511 costs $195.00, and the prices on the 8086, Z8000 and the 68000 have not been released. However, it has been rumored that the prices for the 8086 will be in the $10-20 range for 100 lot quantization. Texas Instruments is offering a competitive processor, the 9940, which has 2 k-bytes of ROM on chip, that will also sell for about $10. The primary disadvantage with the 9940 is I/O is serial which greatly reduces its utility for this application.

Conclusion

It is recommended that major effort be spent in the area of algorithm improvement, scientific function speed improvement (sine, cosine, exponentials, etc.), and the total integrated GPS software analysed from the standpoint of overall processor requirements. Considerable progress is occurring at a rapid rate in the area of microprocessor design. The full 24 GPS satellites will not be operational until 1985. It is believed that this study has shown that the microprocessor state-of-the-art is changing so rapidly that the low-cost designer is best advised to hold off as long as possible to select the best microprocessor for his receiver. In the interim, the basic software algorithms can be meticulously organized, programmed, and tested in a higher order language. In addition, simulations can be performed to evaluate the receiver/processor interface performance. As a final step, a specific microprocessor can be interfaced with the system.

Most military software specifications require that the software is written in a top-down structured high order language. This requirement alone implies the need for a microprocessor development system that can translate the high order language. This requirement may indeed prove to be the best approach for a low-cost GPS receiver/processor also.